VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims presently in the application as follows:

2. (Twice Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of the semiconductor device on a same plane.

3. (Twice Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and

said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of the semiconductor device on a same plane.

9. (Twice Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of said semiconductor device on a same plane.